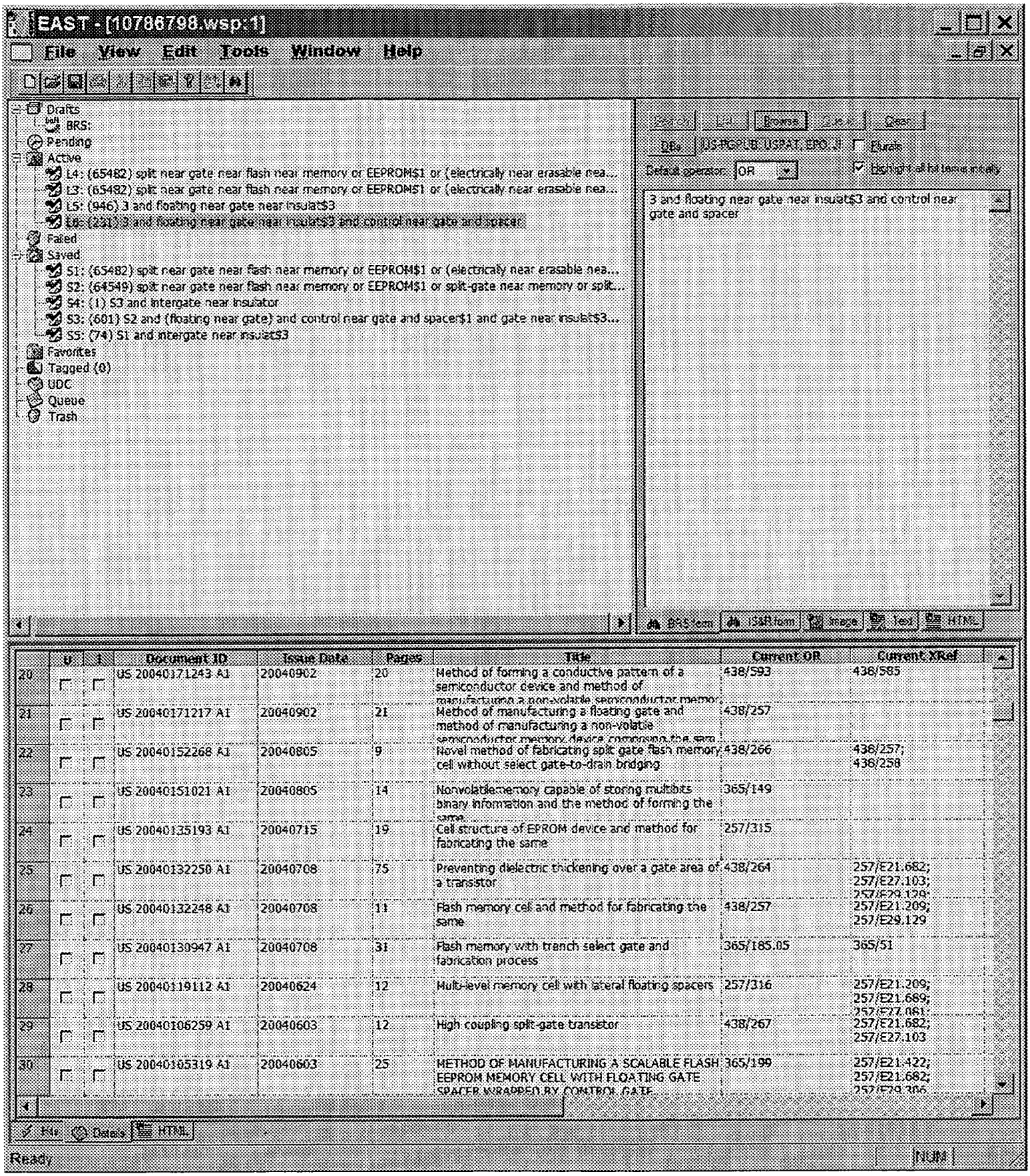

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
20	☐	☐	US 20040171243 A1	20040902	20	Method of forming a conductive pattern of a semiconductor device and method of manufacturing a non-volatile semiconductor memor	438/593	438/585
21	☐	☐	US 20040171217 A1	20040902	21	Method of manufacturing a floating gate and method of manufacturing a non-volatile semiconductor memory device comprising the sam	438/257	
22	☐	☐	US 20040152268 A1	20040805	9	Novel method of fabricating split gate flash memory cell without select gate-to-drain bridging	438/266	438/257; 438/258
23	☐	☐	US 20040151021 A1	20040805	14	Nonvolatilememory capable of storing multibits binary information and the method of forming the same	365/149	
24	☐	☐	US 20040135193 A1	20040715	19	Cell structure of EPROM device and method for fabricating the same	257/315	
25	☐	☐	US 20040132250 A1	20040708	75	Preventing dielectric thickening over a gate area of a transistor	438/264	257/E21.682; 257/E27.103; 257/E29.129;
26	☐	☐	US 20040132248 A1	20040708	11	Flash memory cell and method for fabricating the same	438/257	257/E21.209; 257/E29.129
27	☐	☐	US 20040130947 A1	20040708	31	Flash memory with trench select gate and fabrication process	365/185.05	365/51
28	☐	☐	US 20040119112 A1	20040624	12	Multi-level memory cell with lateral floating spacers	257/316	257/E21.209; 257/E21.689; 257/E27.081;
29	☐	☐	US 20040106259 A1	20040603	12	High coupling split-gate transistor	438/267	257/E21.682; 257/E27.103
30	☐	☐	US 20040105319 A1	20040603	25	METHOD OF MANUFACTURING A SCALABLE FLASH EEPROM MEMORY CELL WITH FLOATING GATE SPACER WRAPPED BY CONTROL GATE	365/199	257/E21.422; 257/E21.682; 257/E29.306